a filter disposed between the input terminal and the output terminal to provide a substantially DC voltage at the output terminal, the filter including at least one element connecting the intermediate terminal to the output terminal.

2. The voltage regulator of claim 1, wherein the first transistor is a PMOS transistor and the second transistor is an NMOS transistor.

3. The voltage regulator of claim 2, wherein the first gate voltage is larger than the second gate voltage.

4. The voltage regulator of claim 3, wherein the first gate voltage is substantially equal to an input voltage at the input terminal.

5. The voltage regulator of claim 3, wherein the second gate voltage is compatible with a logic voltage.

6. The voltage regulator of claim 5, wherein the first gate voltage is greater than the logic voltage.

7. The voltage regulator of claim 3, wherein the first gate oxide layer is thicker than the second gate oxide layer.

8. The voltage regulator of claim 1, wherein the controller includes a first plurality of transistors in a drive train of the first transistor and a second plurality of transistors in a drive train of the second transistor.

9. The voltage regulator of claim 8, wherein the second plurality of transistors are driven with the second gate voltage.

10. The voltage regulator of claim 8, wherein the first plurality of transistors includes a third transistor driven with the first gate voltage and a fourth transistor driven with the second gate voltage.

11. A voltage regulator having an input terminal and an output terminal, comprising:

a transistor to intermittently couple the input terminal to the output terminal, wherein the transistor includes a source, a drain, and a gate, and the transistor has a channel length between the source and the drain which is less than a channel length required for reliable behavior under steady state saturation conditions; and

a filter disposed between the input terminal and the output terminal to provide a substantially DC voltage at the output terminal.

12. The voltage regulator of claim 11, wherein the channel length is about 1 micron.

13. The voltage regulator of claim 11, wherein the channel length is shorter than a channel length specified for standard hot electron specification of 10% degradation in a one year period of operation.

14. The voltage regulator of claim 11, wherein the transistor is fabricated using one or more of process proximity correction and phase shift mask technology.

15. A voltage regulator having an input terminal and an output terminal, comprising:

a first transistor connecting the input terminal to an intermediate terminal, the first transistor including a first gate oxide layer;

a second transistor connecting the intermediate terminal to ground, the second transistor including a second gate oxide layer that is thinner than the first gate oxide layer;

a controller that drives the first and second transistors to alternately couple the intermediate terminal between the input terminal and ground; and

a filter disposed between the input terminal and the output terminal to provide a substantially DC voltage at the output terminal, the filter including at least one element connecting the intermediate terminal to the output terminal.

16. The voltage regulator of claim 15, wherein the first transistor is a PMOS transistor and the second transistor is an NMOS transistor.

17. The voltage regulator of claim 16, wherein the controller drives the first transistor with a first gate voltage and drives the second transistor with a second, different gate voltage.

18. (Amended) The voltage regulator of claim 17, wherein the first gate voltage is larger than the second gate voltage.

19. A voltage regulator having an input terminal and an output terminal, comprising:

a first transistor connecting the input terminal to an intermediate terminal;

a second transistor connecting the intermediate terminal to ground;

a controller that drives the first and second transistors to alternately couple the intermediate terminal between the input terminal and ground, wherein the controller drives the first transistor with a first gate voltage and drives the second transistor with a second, different gate voltage; and

a filter disposed between the input terminal and the output terminal to provide a substantially DC voltage at the output terminal, the filter including at least one element connecting the intermediate terminal to the output terminal;

wherein the first transistor includes a source, a drain and a gate, and the first transistor has a channel length between the source and the drain which is less than a channel length required for reliable behavior under steady state saturation conditions.

20. A voltage regulator having an input terminal and an output terminal, comprising:

a first transistor connecting the input terminal to an intermediate terminal;

a second transistor connecting the intermediate terminal to ground;

a controller that drives the first and second transistors to alternately couple the intermediate terminal between the input terminal and ground, wherein the controller drives the first transistor with a first gate voltage and drives the second transistor with a second, different gate voltage; and

a filter disposed between the input terminal and the output terminal to provide a substantially DC voltage at the output terminal, the filter including at least one element connecting the intermediate terminal to the output terminal;

wherein the second transistor includes a source, a drain and a gate, and the second transistor has a channel length between the source and the drain which is less than a channel length required for reliable behavior under steady state saturation conditions.

21. The voltage regulator of claim 1, wherein the first and second transistors have a double diffused drain structure.

22. The voltage regulator of claim 1, wherein the first and second oxide layers are formed on a surface of a semiconductor.

23. The voltage regulator of claim 1, wherein application of the first gate voltage turns the first transistor on.

24. The voltage regulator of claim 1, wherein application of the second gate voltage turns the second transistor on.

REMARKS

I. Indefiniteness

Claim 18 stands rejected as indefinite on the grounds of improper antecedent basis. Applicant believes the present amendment addresses the Examiner's concerns.

II. Restriction

Applicant thanks the Examiner for the telephone conference of April 3, 2001.